## AMENDMENTS TO THE CLAIMS

1-20. (Canceled)

21. (Previously Presented) An electrode structure, comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, said dielectric having an opening exposing a portion of said first conductive layer;

an adhesion layer in said opening in said dielectric layer and over said exposed portion of said first conductive layer;

a second conductive layer formed at least partially over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening in said dielectric layer; and

a third conductive layer formed over and at least partially in contact with said second conductive layer and said adhesion layer within said opening.

22. (Currently Amended) The electrode structure of claim 21, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

23. (Currently Amended) The electrode structure of claim 21, wherein said third conductive layer is patterned.

24. (Currently Amended) The electrode structure of claim 21, wherein said adhesion layer comprises an oxide or a nitride.

25. (Currently Amended) The electrode structure of claim 21, wherein said adhesion layer comprises titanium nitride.

26. (Currently Amended) The electrode structure of claim 21, wherein said first conductive layer comprises at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

27. (Currently Amended) The electrode structure of claim 21, wherein said second conductive layer comprises tungsten.

28. (Currently Amended) The electrode structure of claim 21, wherein said third conductive layer is formed from a same material as the first conductive material.

29. (Currently Amended) The electrode structure of claim 21, wherein said third conductive layer is formed from a same material as the second conductive material.

30. (Withdrawn-Currently Amended) A resistance variable memory device, comprising:

a variable resistance memory element formed over an electrode structure, said electrode structure comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, ~~wherein~~ said dielectric having an opening ~~in said dielectric exposes~~ exposing a portion of said first conductive layer;

an adhesion layer ~~over~~ in said opening in said dielectric layer and over said exposed portion of said first conductive layer;

a second conductive layer formed at least partially over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening in said dielectric layer;

a third conductive layer ~~over said dielectric layer and over~~ formed over and at least partially in contact with said second conductive layer and said adhesion layer within said opening; and

a fourth conductive layer formed over said variable resistance memory element.

31. (Withdrawn) The resistance variable memory device of claim 30, wherein said variable resistance memory element is a chalcogenide glass having metal ions dissolved therein.

32. (Withdrawn) The resistance variable memory device of claim 30, wherein said variable resistance memory element is a molecular memory element.

33. (Withdrawn) The method of claim 30, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

34. (Withdrawn) The resistance variable memory device claim 30, wherein said third conductive layer is patterned.

35. (Withdrawn) The resistance variable memory device of claim 30, wherein said adhesion layer comprises one of an oxide and a nitride.

36. (Withdrawn) The resistance variable memory device of claim 30, wherein said adhesion layer comprises titanium nitride.

37. (Withdrawn) The resistance variable memory device of claim 30, wherein said first conductive layer comprises at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

38. (Withdrawn) The resistance variable memory device of claim 30 wherein said second conductive layer comprises tungsten.

39. (Withdrawn) The resistance variable memory device of claim 30, wherein said third conductive layer comprises a same material as the first conductive layer.

40. (Withdrawn) The resistance variable memory device of claim 30, wherein said third conductive layer comprises a same material as the second conductive layer.

41. (Withdrawn-Currently Amended) A memory system, comprising:

an array of memory devices, each memory device ~~having an electrode structure~~ comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, ~~wherein~~ said dielectric having an opening ~~in said dielectric exposes~~ exposing a portion of said first conductive layer;

an adhesion layer ~~over~~ in said opening in said dielectric layer and over said exposed portion of said first conductive layer;

a second conductive layer formed at least partially over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening in said dielectric layer;

a third conductive layer ~~over said dielectric layer,~~ formed over and at least partially in contact with said second conductive layer and said adhesion layer within said opening; ~~and~~

a variable resistance memory element formed over an in contact with said third conductive layer; and

a fourth conductive layer formed over and in contact with said variable resistance memory element.

42. (Canceled)

43. (Withdrawn) The memory system of claim 42, wherein said variable resistance memory element is a chalcogenide glass having metal ions dissolved therein.

44. (Withdrawn) The memory system of claim 42, wherein said variable resistance memory element is a molecular memory element.

45. (Withdrawn) The memory system of claim 41, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

46. (Withdrawn) The memory system of claim 41, wherein said third conductive layer is patterned.

47. (Withdrawn) The memory system of claim 41, wherein said adhesion layer comprises one of an oxide and a nitride.

48. (Withdrawn) The memory system of claim 41, wherein said adhesion layer comprises titanium nitride.

49. (Withdrawn) The memory system of claim 41, wherein said first conductive layer is formed from at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

50. (Withdrawn) The memory system of claim 43, wherein said second conductive layer comprises tungsten.

51. (Withdrawn) The memory system of claim 43, wherein said third conductive layer comprises a same material as the first conductive layer.

52. (Withdrawn) The memory system of claim 43, wherein said third conductive layer comprises a same material as the second conductive layer.

53. (Withdrawn-Currently Amended) A processor system, comprising:

a processor; and

a memory circuit electrically coupled to said processor, said memory circuit having an electrode structure comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, ~~wherein~~ said dielectric having an opening ~~in said dielectric exposes~~ exposing a portion of said first conductive layer;

an adhesion layer ~~over~~ in said opening in said dielectric layer and over said exposed portion of said first conductive layer;

a second conductive layer ~~over~~ formed at least partially over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening in said dielectric layer;

a third conductive layer ~~over said dielectric layer,~~ formed over and at least partially in contact with said second conductive layer and said adhesion layer within said opening.

54. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

55. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said third conductive layer is patterned.

56. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said adhesion layer comprises an oxide or a nitride.

57. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said adhesion layer comprises titanium nitride.

58. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said third conductive layer is formed from a same material as the first conductive material.

59. (Withdrawn-Currently Amended) The ~~electrode~~ processor system of claim 53, wherein said third conductive layer is formed from a same material as the second conductive material.